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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/587,496 | 06/02/2000 | Brian Bailey | | 7286 |

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| EXAMINER | |
|---|---|
| SHARON, AYAL I | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2123 | |

DATE MAILED: 02/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/587,496 | BAILEY ET AL. | |
| | Examiner | Art Unit | |
| | Ayal I Sharon | 2123 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *1/11/2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,2,4-8,10-23 and 26-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-2,4,10,14,18,20-23,26,28-30,33-42* is/are rejected.

7)☒ Claim(s) *5-8,11-13,15-17,19,27,31 and 32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 June 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Introduction*

1. Claims 1-2, 4-8, 10-23 and 26-42 of U.S. Application 09/587,496, originally filed on 06/02/2000 are presented for examination. Applicant's RCE, filed 1/11/2005, amended claims 1, 13, 20, 21, 22, 23, and 26. Claims 3, 9, and 24-25 have been cancelled. Claims 26-42 have been added.
2. Examiner notes that Claim 26 is marked as "currently amended" but is a new claim.

### *Drawings*

3. The draftsperson has objected to the drawings submitted on 06/02/0000. Please see form PTO-948, mailed with the first Office Action, for details of the objections.

### *Claim Objections*

4. Claims 5-8, 11-13, 15-17, 19, 27 and 31-32 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and all intervening claims.

***Claim Rejections - 35 USC § 102***

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. The prior art used for these rejections is as follows:

7. Hellestrand et al. U.S. Patent 6,263,302. (Henceforth referred to as "**Hellestrand**").

8. The claim rejections are hereby summarized for Applicant's convenience. The detailed rejections follow.

9. **Claims 1-2, 4, 10, 14, 18, 20–23, 26, 28-30, and 33-42 are rejected under 35 U.S.C. 102(e) as being anticipated by Hellestrand.**

10. In regards to claim 1, Hellestrand teaches the following limitations:

1. (Currently amended) A method comprising: retrieving state configuration information from a state server of a hardware/software co-simulation, the hardware/software co-simulation comprising:
simulation of at least one memory device by a logic simulator, the logic simulator comprising a memory interface model and a memory store;
(Hellestrand, especially: Fig.1 and col.10, lines 15-35)

Examiner interprets that Applicant's "logic simulator" corresponds to Hellestrand's "Description of Target Circuitry" (Item 105, Fig.1).

Examiner interprets that Applicant's "memory interface model" corresponds to Hellestrand's "Memory model" (Item 122, Fig.1).

Examiner interprets that Applicant's "memory store" corresponds to Hellestrand's "host computer system" (col.10, lines 15-24). Hellestrand teaches (col.10, lines

15-24) that "... the hardware simulator provides for simulating at least some of the operations of the target memory by running a hardware model 122 of the target memory, with the contents of the simulated target memory stored in the host computer system."

simulation of a microprocessor at least in part by a first bus interface model, the simulation of the microprocessor executing software stored in the simulation of the at least one memory device;
(Hellestrand, especially: Fig.1 and col.9, lines 52-62 and col.10, lines 24-48)

Examiner interprets that Applicant's "bus interface model" corresponds to Hellestrand's "Bus model" (Item 124, Fig.1).

Examiner interprets that Applicant's "... software stored in the simulation of the at least one memory device" corresponds to Hellestrand's "Analyzed version of the user program" (Item 111, Fig.1 and col.9, lines 52-62).

Hellestrand teaches (col.9, lines 52-56) that "Processor simulator 107 simulates execution of a user program 109 on the target processor by executing an analyzed version of the user program 111 of the user program 109."

a first kernel managing access to the memory store; and
(Hellestrand, especially: Fig.1 and col.9, line 65 to col.10, line 4)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

a second kernel comprising a co-simulation manager and a memory manager; and providing a client of the hardware/software co-simulation access to a server state of the state server based on the state configuration information, wherein the state configuration information comprises memory mapping, symbol allocation, and symbol type.
(Hellestrand, especially: Fig.1 and col.9, lines 52 to col.10, line 15)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

Hellestrand teaches (col.9, line 65 to col.10, line 4) that "... the processor simulator includes ... a memory mapper 125 that translates between host memory addresses and target memory addresses using memory mapping information 108 relating host addresses to target addresses."

Hellestrand also teaches the use of a "memory allocation simulator" (Item 123, Fig.1). Hellestrand teaches (col.11, lines 10-30) that "In the case the processor simulator includes the memory allocation simulator 123, analysis further includes inserting hooks in the user program to invoke the memory allocation simulator...".

Examiner interprets that these "hooks" correspond to symbol allocation and symbol type info.

11. In regards to claim 2, Hellestrand teaches the following limitations:

2. (Original) The method of claim 1 wherein the state server defines an address space or a virtual address space in the hardware/software co-simulation.
(Hellestrand, especially: Fig.1 and col.9, lines 52 to col.10, line 15)

Hellestrand teaches (col.9, line 65 to col.10, line 4) that "... the processor simulator includes ... a memory mapper 125 that translates between host memory addresses and target memory addresses using memory mapping information 108 relating host addresses to target addresses."

12. In regards to claim 4,

4. (Original) The method of claim 1 further comprising: registering the client with a co-simulation interface; and associating the client with at least one state server in the hardware/software co--simulation.
(Hellestrand, especially: col.10, lines 4-14)

Hellestrand teaches (col.10, lines 4-14) that "An interface mechanism 119 is coupled to both the processor simulator 107 and the hardware simulator 103 and enables communication between processor simulator 107 and the hardware simulator 103. Processor simulator 107 includes a communication mechanism 141 to pass information to the hardware simulator 103 using the interface mechanism when an event requires interaction of user program 109 with the target digital circuitry."

13. In regards to claim 10,

10. (Original) The method of claim 1 further comprising: requesting the state configuration information, said state configuration information to define at least one memory location comprising the server state.
(Hellestrand, especially: col.9, line 60 to col.10, line 4)

Hellestrand teaches that (col.9, line 60 to col.10, line 4) "...the processor simulator 107 generates accurate execution timing information incorporating the target processor instruction timing ..." and "Furthermore, for a processor that includes a cache, the processor simulator includes a cache simulator 121 executing a cache model, and a memory mapper 125 ..."

14. In regards to claim 14,

14. (Original) The method of claim 1 wherein providing the client access comprises: performing a memory operation on at least one memory location based on the state configuration information.
(Hellestrand, especially: col.9, line 60 to col.10, line 4)

Hellestrand teaches that (col.9, line 60 to col.10, line 4) "...the processor simulator 107 generates accurate execution timing information incorporating the target processor instruction timing ..." and "Furthermore, for a processor that includes a cache, the processor simulator includes a cache simulator 121 executing a cache model, and a memory mapper 125 that translates between host memory addresses and target memory addresses using memory mapping information 108 relating host addresses to target addresses."

Examiner finds the act of performing a memory operation on a memory location Based on state configuration information to be inherent, because changing the values of stored variables always involve a overwriting the recorded value.

15. In regards to claim 18,

18. (Original) The method of claim 1 further comprising:

receiving stimulus based on the server state;
and applying the stimulus to the hardware/software co-simulation.
(Hellestrand, especially: col.9, line 60 to col.10, line 4)

Hellestrand teaches that (col.9, line 60 to col.10, line 4) "...the processor simulator 107 generates accurate execution timing information incorporating the target processor instruction timing ..." and "Furthermore, for a processor that includes a cache, the processor simulator includes a cache simulator 121 executing a cache model, and a memory mapper 125 that translates between host memory addresses and target memory addresses using memory mapping information 108 relating host addresses to target addresses."

16. In regards to claim 20, Hellestrand teaches the following limitations:

20. (Currently amended) A method comprising: accessing a software state from a hardware simulation process in a hardware/software co-simulation, the hardware/software co-simulation comprising:
(Hellestrand, especially: Fig.1 and col.10, lines 15-35)

simulation of at least one memory device by a logic simulator, the logic simulator comprising a memory interface model and a memory store;
(Hellestrand, especially: Fig.1 and col.10, lines 15-35)

Examiner interprets that Applicant's "logic simulator" corresponds to Hellestrand's "Description of Target Circuitry" (Item 105, Fig.1).

Examiner interprets that Applicant's "memory interface model" corresponds to Hellestrand's "Memory model" (Item 122, Fig.1).

Examiner interprets that Applicant's "memory store" corresponds to Hellestrand's "host computer system" (col.10, lines 15-24). Hellestrand teaches (col.10, lines 15-24) that "... the hardware simulator provides for simulating at least some of the operations of the target memory by running a hardware model 122 of the target memory, with the contents of the simulated target memory stored in the host computer system."

simulation of a microprocessor at least in part by a first bus interface model, the simulation of the microprocessor executing software stored in the simulation of the at least one memory device;
(Hellestrand, especially: Fig.1 and col.9, lines 52-62 and col.10, lines 24-48)

Examiner interprets that Applicant's "bus interface model" corresponds to Hellestrand's "Bus model" (Item 124, Fig.1).

Examiner interprets that Applicant's "... software stored in the simulation of the at least one memory device" corresponds to Hellestrand's "Analyzed version of the user program" (Item 111, Fig.1 and col.9, lines 52-62).

Hellestrand teaches (col.9, lines 52-56) that "Processor simulator 107 simulates execution of a user program 109 on the target processor by executing an analyzed version of the user program 111 of the user program 109."

a first kernel managing access to the memory store; and
(Hellestrand, especially: Fig.1)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

a second kernel comprising a co-simulation manager and a memory manager; and providing access to the software state to a client of the hardware/software co-simulation.
(Hellestrand, especially: Fig.1 and col.9, lines 52 to col.10, line 15)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

Hellestrand teaches (col.9, line 65 to col.10, line 4) that "... the processor simulator includes ... a memory mapper 125 that translates between host memory addresses and target memory addresses using memory mapping information 108 relating host addresses to target addresses."

Hellestrand also teaches the use of a "memory allocation simulator" (Item 123, Fig.1). Hellestrand teaches (col.11, lines 10-30) that "In the case the processor simulator includes the memory allocation simulator 123, analysis further includes inserting hooks in the user program to invoke the memory allocation simulator...".

Examiner interprets that these "hooks" correspond to symbol allocation and symbol type info.

17. In regards to claim 21, Hellestrand teaches the following limitations:

21. (Currently amended) A machine readable storage medium having stored thereon machine executable instructions, execution of said machine executable instructions to implement a method comprising:
(Hellestrand, especially: Fig.1 and col.10, lines 15-35)

retrieving state configuration information from a state server of a hardware/software co-simulator, the hardware/software co-simulator comprising:
(Hellestrand, especially: Fig.1 and col.9 lines 52-63)

Hellestrand teaches (col.10, lines 7-11) that "Processor simulator 107 simulates execution of a user program 109 on the target processor by executing an analyzed version of the user program 111 of the user program 109. ... The analyzed version includes the user program, and timing information on how the target processor would execute the user program 109 such that while the host processor executes the analyzed version 111 of the user program, the processor simulator 107 generates accurate execution timing information incorporating the target processor instruction timing as if the user program 109 was executing on the target processor."

Examiner interprets that this "timing information" is a form of state configuration configuration information.

simulation of at least one memory device by a logic simulator, the logic simulator comprising a memory interface model and a memory store;
(Hellestrand, especially: Fig.1 and col.10, lines 15-35)

Examiner interprets that Applicant's "logic simulator" corresponds to Hellestrand's "Description of Target Circuitry" (Item 105, Fig.1).

Examiner interprets that Applicant's "memory interface model" corresponds to Hellestrand's "Memory model" (Item 122, Fig.1).

Examiner interprets that Applicant's "memory store" corresponds to Hellestrand's "host computer system" (col.10, lines 15-24). Hellestrand teaches (col.10, lines 15-24) that "... the hardware simulator provides for simulating at least some of the operations of the target memory by running a hardware model 122 of the target memory, with the contents of the simulated target memory stored in the host computer system."

simulation of a microprocessor at least in part by a first bus interface model, the simulation of the microprocessor executing software stored in the simulation of the at least one memory device;

(Hellestrand, especially: Fig.1 and col.9, lines 52-62 and col.10, lines 24-48)

Examiner interprets that Applicant's "bus interface model" corresponds to Hellestrand's "Bus model" (Item 124, Fig.1).

Examiner interprets that Applicant's "... software stored in the simulation of the at least one memory device" corresponds to Hellestrand's "Analyzed version of the user program" (Item 111, Fig.1 and col.9, lines 52-62).

Hellestrand teaches (col.9, lines 52-56) that "Processor simulator 107 simulates execution of a user program 109 on the target processor by executing an analyzed version of the user program 111 of the user program 109."

a first kernel managing access to the memory store; and
(Hellestrand, especially: Fig.1 and col.9, line 65 to col.10, line 4)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

a second kernel comprising a co-simulation manager and a memory manager; and providing a client of the hardware/software co-simulation access to a server state of the state server based on the state configuration information, wherein the state configuration information comprises memory mapping, symbol allocation, and symbol type.
(Hellestrand, especially: Fig.1 and col.9, lines 52 to col.10, line 15)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

Hellestrand teaches (col.9, line 65 to col.10, line 4) that "... the processor simulator includes ... a memory mapper 125 that translates between host memory addresses and target memory addresses using memory mapping information 108 relating host addresses to target addresses."

Hellestrand also teaches the use of a "memory allocation simulator" (Item 123, Fig.1). Hellestrand teaches (col.11, lines 10-30) that "In the case the processor simulator includes the memory allocation simulator 123, analysis further includes inserting hooks in the user program to invoke the memory allocation simulator...".

Examiner interprets that these "hooks" correspond to symbol allocation and symbol type info.

18. In regards to claim 22, Hellestrand teaches the following limitations:

22. (Currently amended) A machine readable storage medium having stored thereon machine executable instructions, execution of said machine executable instructions to implement a method

comprising: accessing a software state from a hardware simulation process in a hardware/software co-simulation, the hardware/software co-simulation comprising:

simulation of at least one memory device by a logic simulator, the logic simulator comprising a memory interface model and a memory store;

(Hellestrand, especially: Fig.1 and col.10, lines 15-35)

Examiner interprets that Applicant's "logic simulator" corresponds to Hellestrand's "Description of Target Circuitry" (Item 105, Fig.1).

Examiner interprets that Applicant's "memory interface model" corresponds to Hellestrand's "Memory model" (Item 122, Fig.1).

Examiner interprets that Applicant's "memory store" corresponds to Hellestrand's "host computer system" (col.10, lines 15-24). Hellestrand teaches (col.10, lines 15-24) that "... the hardware simulator provides for simulating at least some of the operations of the target memory by running a hardware model 122 of the target memory, with the contents of the simulated target memory stored in the host computer system."

simulation of a microprocessor at least in part by a first bus interface model, the simulation of the microprocessor executing software stored in the simulation of the at least one memory device;

(Hellestrand, especially: Fig.1 and col.9, lines 52-62 and col.10, lines 24-48)

Examiner interprets that Applicant's "bus interface model" corresponds to Hellestrand's "Bus model" (Item 124, Fig.1).

Examiner interprets that Applicant's "... software stored in the simulation of the at least one memory device" corresponds to Hellestrand's "Analyzed version of the user program" (Item 111, Fig.1 and col.9, lines 52-62).

Hellestrand teaches (col.9, lines 52-56) that "Processor simulator 107 simulates execution of a user program 109 on the target processor by executing an analyzed version of the user program 111 of the user program 109."

a first kernel manning access to the memory store: and

(Hellestrand, especially: Fig.1 and col.9, line 65 to col.10, line 4)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

a second kernel comprising a co-simulation manager and a memory manager; and providing access to the software state to a client of the hardware/software co-simulation.

(Hellestrand, especially: Fig.1 and col.9, lines 52 to col.10, line 15)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

Hellestrand teaches (col.9, line 65 to col.10, line 4) that "... the processor simulator includes ... a memory mapper 125 that translates between host memory addresses and target memory addresses using memory mapping information 108 relating host addresses to target addresses."

Hellestrand also teaches the use of a "memory allocation simulator" (Item 123, Fig.1). Hellestrand teaches (col.11, lines 10-30) that "In the case the processor simulator includes the memory allocation simulator 123, analysis further includes inserting hooks in the user program to invoke the memory allocation simulator...".

Examiner interprets that these "hooks" correspond to symbol allocation and symbol type info.

19. In regards to claim 23, Hellestrand teaches the following limitations:

23. (Currently amended) An apparatus comprising:
a hardware/software co-simulator to retrieve state configuration information from a state server, the hardware/software co-simulator comprising:

simulation of at least one memory device by a logic simulator, the logic simulator comprising a memory interface model and a memory store;
(Hellestrand, especially: Fig.1 and col.10, lines 15-35)

Examiner interprets that Applicant's "logic simulator" corresponds to Hellestrand's "Description of Target Circuitry" (Item 105, Fig.1).

Examiner interprets that Applicant's "memory interface model" corresponds to Hellestrand's "Memory model" (Item 122, Fig.1).

Examiner interprets that Applicant's "memory store" corresponds to Hellestrand's "host computer system" (col.10, lines 15-24). Hellestrand teaches (col.10, lines 15-24) that "... the hardware simulator provides for simulating at least some of the operations of the target memory by running a hardware model 122 of the target memory, with the contents of the simulated target memory stored in the host computer system."

simulation of a microprocessor at least in part by a first bus interface model, the simulation of the microprocessor executing software stored in the simulation of the at least one memory device;
(Hellestrand, especially: Fig.1 and col.9, lines 52-62 and col.10, lines 24-48)

Examiner interprets that Applicant's "bus interface model" corresponds to Hellestrand's "Bus model" (Item 124, Fig.1).

Examiner interprets that Applicant's "... software stored in the simulation of the at least one memory device" corresponds to Hellestrand's "Analyzed version of the user program" (Item 111, Fig.1 and col.9, lines 52-62).

Hellestrand teaches (col.9, lines 52-56) that "Processor simulator 107 simulates execution of a user program 109 on the target processor by executing an analyzed version of the user program 111 of the user program 109."

a first kernel managing access to the memory store; and
(Hellestrand, especially: Fig.1 and col.9, line 65 to col.10, line 4)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

a second kernel comprising a co-simulation manager and a memory manager; and
(Hellestrand, especially: Fig.1 and col.9, lines 52 to col.10, line 15)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

Hellestrand teaches (col.9, line 65 to col.10, line 4) that "... the processor simulator includes ... a memory mapper 125 that translates between host memory addresses and target memory addresses using memory mapping information 108 relating host addresses to target addresses."

Hellestrand also teaches the use of a "memory allocation simulator" (Item 123, Fig.1). Hellestrand teaches (col.11, lines 10-30) that "In the case the processor simulator includes the memory allocation simulator 123, analysis further includes inserting hooks in the user program to invoke the memory allocation simulator...".

Examiner interprets that these "hooks" correspond to symbol allocation and symbol type info.

a unified memory store, said hardware/software co-simulator to provide a client access to a server state of the state server within the unified memory store based on the state configuration information.
(Hellestrand, especially: Fig.1 and col.9, lines 52-62 and col.10, lines 24-48)

Examiner interprets that Applicant's "bus interface model" corresponds to Hellestrand's "Bus model" (Item 124, Fig.1).

Examiner interprets that Applicant's "... software stored in the simulation of the at least one memory device" corresponds to Hellestrand's "Analyzed version of the user program" (Item 111, Fig.1 and col.9, lines 52-62).

Hellestrand teaches (col.9, lines 52-56) that "Processor simulator 107 simulates execution of a user program 109 on the target processor by executing an analyzed version of the user program 111 of the user program 109."

20. In regards to claim 26, Hellestrand teaches the following limitations:

26. (Currently amended) The method of claim 1, wherein the memory mapping comprises a plurality of memory addresses corresponding to the server state.
(Hellestrand, especially: Fig.1 and col.9, lines 52 to col.10, line 15)

Examiner interprets that Applicant's two "kernels" correspond to Hellestrand's "memory mapper" (Item 125, Fig.1).

Hellestrand teaches (col.9, line 65 to col.10, line 4) that "... the processor simulator includes ... a memory mapper 125 that translates between host memory addresses and target memory addresses using memory mapping information 108 relating host addresses to target addresses."

21. In regards to claim 28, Hellestrand teaches the following limitations:

28. (New) The method of claim 1, wherein the state server comprises at least one component that contains and allows for exporting of the state configuration information to the client.
(Hellestrand, especially: col.9, line 22 to col.11, line 31)

22. In regards to claim 29, Hellestrand teaches the following limitations:

29. (New) The method of claim 1, wherein the state server comprises a hardware process.
(Hellestrand, especially: col.9, line 22 to col.11, line 31)

23. In regards to claim 30, Hellestrand teaches the following limitations:

30. (New) The method of claim 1, wherein the state server comprises a software process.
(Hellestrand, especially: col.9, line 22 to col.11, line 31)

24. In regards to claim 33, Hellestrand teaches the following limitations:

33. (New) The method of claim 1, wherein the memory interface model represents input and output behavior of the at least one memory device.
(Hellestrand, especially: col.9, line 22 to col.11, line 31)

25. In regards to claim 34, Hellestrand teaches the following limitations:

34. (New) The method of claim 1, wherein the simulation of the microprocessor comprises simulation at least in part by a first instruction set simulator.
(Hellestrand, especially: col.9, line 22 to col.11, line 31)

26. In regards to claim 35, Hellestrand teaches the following limitations:

35. (New) The method of claim 34, wherein the first bus interface model represents input and output behavior of the simulation of the microprocessor.
(Hellestrand, especially: col.9, line 22 to col.11, line 31)

27. In regards to claim 36, Hellestrand teaches the following limitations:

36. (New) The method of claim 34, wherein the co-simulation manager monitors transactions between the first instruction set simulator and the first bus interface model.
(Hellestrand, especially: col.9, line 22 to col.11, line 31)

28. In regards to claim 37, Hellestrand teaches the following limitations:

37. (New) The method of claim 1, wherein the first kernel and second kernel are the same kernel.
(Hellestrand, especially: col.9, line 22 to col.11, line 31)

29. In regards to claim 38, Hellestrand teaches the following limitations:

38. (New) The method of claim 34, wherein the hardware/software co-simulation further comprises a simulation of a digital signal processor, the digital signal processor having a corresponding address space and a corresponding symbol table.
(Hellestrand, especially: col.9, line 22 to col.11, line 31)

Examiner finds this the "simulation of a digital signal processor" to be a case of intended use.

30. In regards to claim 39, Hellestrand teaches the following limitations:

39. (New) The method of claim 38, wherein the simulation of the digital signal processor comprises simulation at least in part by a second instruction set simulator and a second bus interface model.
(Hellestrand, especially: col.9, line 22 to col.11, line 31)

31. In regards to claim 40, Hellestrand teaches the following limitations:

40. (New) The method of claim 34, wherein the hardware/software co-simulation further comprises a simulation of a generic co-simulation client, the generic co-simulation client having a corresponding address space and a corresponding symbol table.
(Hellestrand, especially: col.9, line 22 to col.11, line 31)

32. In regards to claim 41, Hellestrand teaches the following limitations:

41. (New) The method of claim 40, wherein the generic co-simulation client is simulated by a second instruction set simulator and a second bus interface model.
(Hellestrand, especially: col.9, line 22 to col.11, line 31)

33. In regards to claim 42, Hellestrand teaches the following limitations:

.42. (New) The method of claim 1, wherein the memory manager manages access to the memory store by the second kernel.
(Hellestrand, especially: col.9, line 22 to col.11, line 31)

***Correspondence Information***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ayal I. Sharon whose telephone number is (571) 272-3714. The examiner can normally be reached on Monday through Thursday, and the first Friday of a biweek, 8:30 am – 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached at (571) 272-3716.

Any response to this office action should be faxed to (703) 872-9306 or mailed to:

Director of Patents and Trademarks
Washington, DC 20231

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Tech Center 2100 Receptionist, whose telephone number is (571) 272-2100.

Ayal I. Sharon

Art Unit 2123

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